## Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

### Listing of Claims

1 (Previously Presented): A bias generator for testing of a static random access memory (SRAM) comprising:

an output of the bias generator; and

means for adjusting a set of available magnitudes of a bias voltage output signal at the output using metal programming.

2 (Original): The bias generator of Claim 1, wherein the bias voltage output signal biases a gate of a weak write pull-down transistor of a write driver in the SRAM with a target magnitude predetermined for the SRAM.

3 (Original): The bias generator of Claim 1, wherein the means for adjusting comprises a metal-programmable transistor in the bias generator, the metal-programmable transistor comprising either or both of a metal-programmable pull-up transistor and a metal-programmable pull-down transistor that change one or both of a range and a resolution of the set of available magnitudes when the metal-programmable transistor is metal programmed.

4 (Original): The bias generator of Claim 3, further comprising:

a pull-up array of transistors connected between a first supply voltage and the bias generator output;

a pull-down transistor connected between the bias generator output and a second supply voltage; and

a gate bias circuit connected between a mode select input and a gate of the pull-down transistor,

wherein the metal-programmable pull-up transistor is connectable in parallel or in series with the pull-up transistor array, and

wherein the metal-programmable pull-down transistor is connectable in parallel or in series with the pull-down transistor.

5 (Original): The bias generator of Claim 4, wherein each of the metal-programmable pull-up transistor and the metal-programmable pull-down transistor has a respective ON state resistance that, when either or both are metal programmed, combines with an effective ON state resistance of the pull-up transistor array and an ON state resistance of the pull-down transistor to adjust the set of available magnitudes.

6 (Original): A bias generator for testing of a static random access memory (SRAM) comprising:

a metal-programmable transistor that adjusts a set of available magnitudes of a bias voltage output signal at the bias generator output when metal programmed.

7 (Original): The bias generator of Claim 6, further comprising:

a pull-up array of transistors connected between a first supply voltage and the bias generator output;

a pull-down transistor connected between the bias generator output and a second supply voltage; and

a gate bias circuit connected between a mode select input and a gate of the pull-down transistor,

wherein the metal-programmable transistor is connectable one or both of in series and in parallel with either or both of the pull-up array and the pull-down transistor.

8 (Original): The bias generator of Claim 6, wherein the metal-programmable transistor comprises either or both of a metal-programmable pull-up transistor and a metal-programmable pull-down transistor, the metal-programmable transistor changing one or both of a range and a resolution of the set of available magnitudes when metal programmed.

9 (Previously presented): The bias generator of Claim 8, further comprising:

a mode select input; and

a set of selection inputs,

wherein the mode select input controls a selection between a weak write test mode (WWTM) and a default mode of operation of the bias generator, and wherein the set of selection inputs selects the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic high level at the bias generator output in the default mode.

10 (Original): The bias generator of Claim 8, further comprising:

a first transistor having a source connected to drains of the pull-up transistor array, a drain connected to the bias generator output, and a gate connected to an inverse mode select input; and

a second transistor having a source connected to the second supply voltage, a drain connected to the bias generator output, and a gate connected to the inverse mode select input,

wherein the mode select input and the inverse mode select input control a selection between a weak write test mode (WWTM) and a default mode of operation of the bias generator, a set of selection inputs selecting the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic low level at the bias generator output in the default mode.

11 (Previously presented): The bias generator of Claim 7, wherein the pull-up array transistors are p-type metal oxide semiconductor (PMOS) transistors that function to pull up the bias voltage output signal when in an ON state, and

wherein the pull-down transistor is an n-type metal oxide semiconductor (NMOS) transistor that functions to pull down the bias voltage output signal to the second supply voltage when in the ON state, the second supply voltage being less than the first supply voltage, the second supply voltage optionally being zero volts or a ground voltage.

12 (Original): A metal-programmable weak write test mode (MPWWTM) bias generator for weak write test mode (WWTM) testing of a static random access memory (SRAM) comprising:

a pull-up array of transistors connected between a first supply voltage and an output of the MPWWTM bias generator;

a pull-down transistor connected between the MPWWTM bias generator output and a second supply voltage;

a gate bias circuit connected between a mode select input and a gate of the pull-down transistor; and

a metal-programmable transistor that adjusts a set of available magnitudes of a bias voltage output signal at the MPWWTM bias generator output when metal programmed,

wherein the mode select input controls a selection between a WWTM and a default mode of operation of the MPWWTM bias generator, a set of selection inputs selecting the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic high level at the MPWWTM bias generator output in the default mode.

13 (Original): The MPWWTM bias generator of Claim 12, wherein the pull-up array transistors are connected such that a source of each array transistor is connected to the first supply voltage, a drain of each array transistor is connected to the MPWWTM bias generator output, and a gate of each array transistor except for a gate of a last array transistor is connected to a different selection input of the set of selection inputs, the gate of the last array transistor being connected to the mode select input, and

wherein each of the pull-up array transistors is individually selectable and individually activatable, such that a particular selection and activation of the pull-up array transistors selects a particular magnitude of the set of available magnitudes for the bias voltage output signal in the WWTM.

14 (Original): The MPWWTM bias generator of Claim 13, wherein the particular magnitude of the bias voltage is selected by asserting one or more of the selection inputs of the set that activate respective one or more array transistors of the pull-up array.

15 (Original): The MPWWTM bias generator of Claim 12, wherein the metal-programmable transistor comprises either or both of a metal-programmable pull-up transistor and a metal-programmable pull-down transistor, the metal-programmable pull-up transistor being connectable one or both of in series and in parallel with the pull-up array the metal-programmable pull-down transistor being connectable one or both of in parallel and in series with the pull-down transistor, such that when metal programmed, the metal-programmed transistor changes one or both of a range and a resolution of the set of available magnitudes.

16 (Original): The MPWWTM bias generator of Claim 15, wherein the metal-programmable pull-up transistor connects in parallel with the pull-up transistor array between the first supply voltage and the MPWWTM bias generator output when metal programmed, and

wherein the metal-programmable pull-down transistor connects between the MPWWTM bias generator output and the second supply voltage when metal programmed.

17 (Original): A metal-programmable weak write test mode (MPWWTM) bias generator for weak write test mode (WWTM) testing of a static random access memory (SRAM) comprising:

a pull-up array of transistors connected between a first supply voltage and an output of the MPWWTM bias generator;

a pull-down transistor connected between the MPWWTM bias generator output and a second supply voltage;

a gate bias circuit connected between a mode select input and a gate of the pull-down transistor;

a first transistor having a source connected to drains of the transistors of the pull-up array, a drain connected to the MPWWTM bias generator output, and a gate connected to an inverse mode select input;

a second transistor having a source connected to the second supply voltage, a drain connected to the MPWWTM bias generator output, and a gate connected to the inverse mode select input; and

a metal-programmable transistor that adjusts a set of available magnitudes of a bias voltage output signal at the MPWWTM bias generator output when metal programmed,

wherein the mode select input and the inverse mode select input control a selection between a WWTM and a default mode of operation of the MPWWTM bias generator, a set of selection inputs selecting the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic low level at the MPWWTM bias generator output in the default mode.

18 (Original): The MPWWTM bias generator of Claim 17,wherein the pull-up array transistors are connected such that a source of each array transistor is connected to the first supply voltage, the drain of each array transistor is connected to the source of the first transistor, and a gate of each array transistor is connected to a different selection input of the set of selection inputs, and

wherein each of the pull-up array transistors is individually selectable and individually activatable, such that a particular selection and activation of the pull-up array transistors selects a particular magnitude of the set of available magnitudes for the bias voltage output signal.

19 (Original): The MPWWTM bias generator of Claim 18, wherein the particular magnitude of the bias voltage is selected by asserting one or more of the selection inputs of the set that activate respective one or more array transistors of the array.

20 (Original): The MPWWTM bias generator of Claim 17, wherein the metal-programmable transistor comprises either or both of a metal-programmable pull-up transistor and a metal-programmable pull-down transistor, the metal-programmable

pull-up transistor being connectable one or both of in parallel and in series with the pull-up transistor array, the metal-programmable pull-down transistor being connectable one or both of in parallel and in series with the pull-down transistor, such that when metal programmed, the metal-programmed transistor changes one or both of a range and a resolution of the set of available magnitudes.

21 (Original): A method of modifying a set of available magnitudes of a bias voltage output signal generated by a bias generator comprising:

providing a metal-programmable transistor in the bias generator; and

metal programming the metal-programmable transistor to connect the transistor to circuitry of the bias generator, such that a corresponding ON state resistance of the metal-programmed transistor is combined with an effective ON state resistance of the circuitry to modify the available magnitudes of the set.

22 (Original): The method of modifying of Claim 21, wherein providing a metal-programmable transistor comprises providing either or both of a metal-programmable pull-up transistor and a metal-programmable pull-down transistor in the bias generator, and

wherein metal programming the metal-programmable transistor comprises connecting either or both of the metal-programmable pull-up transistor and the metal-programmable pull-down transistor to the bias generator circuitry.

23 (Original): The method of modifying of Claim 22, wherein metal programming the metal-programmable pull-up transistor to connect to the circuitry combines a corresponding pull-up ON state resistance of the metal-programmed pull-up transistor with an effective ON state resistance of a pull-up transistor array of the bias generator circuitry.

24 (Original): The method of modifying of Claim 22, wherein metal programming the metal-programmable pull-down transistor to connect to the circuitry combines a corresponding pull-down ON state resistance of the metal-programmed pull-down transistor with an ON state resistance of a pull-down transistor of the bias generator circuitry.

25 (Original): The method of modifying of Claim 22, wherein providing a metal-programmable transistor comprises providing either or both of a selection of metal-programmable pull-up transistors and a selection of metal-programmable pull-down transistors in the bias generator, at least one of the metal-programmable transistors of each respective selection being different from other metal-programmable transistors of the respective selections, and

wherein metal programming the metal-programmable transistor comprises selecting a respective metal-programmable transistor from either or both the pull-up transistor selection and the pull-down transistor selection, and connecting the selected respective metal-programmable transistor to the bias generator circuitry.

26 (New): A bias generator for testing of a static random access memory (SRAM) comprising:

a metal-programmable transistor that adjusts a set of available magnitudes of a bias voltage output signal at the bias generator output when metal programmed;

a mode select input; and

a set of selection inputs,

wherein the metal-programmable transistor comprises either or both of a metal-programmable pull-up transistor and a metal-programmable pull-down transistor, the metal-programmable transistor changing one or both of a range and a resolution of the set of available magnitudes when metal programmed, and

wherein the mode select input controls a selection between a weak write test mode (WWTM) and a default mode of operation of the bias generator, and wherein the set of selection inputs selects the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic high level at the bias generator output in the default mode.

27 (New): A bias generator for testing of a static random access memory (SRAM) comprising:

a metal-programmable transistor that adjusts a set of available magnitudes of a bias voltage output signal at the bias generator output when metal programmed;

a first transistor having a source connected to drains of the pull-up transistor array, a drain connected to the bias generator output, and a gate connected to an inverse mode select input; and

a second transistor having a source connected to the second supply voltage, a drain connected to the bias generator output, and a gate connected to the inverse mode select input,

wherein the metal-programmable transistor comprises either or both of a metal-programmable pull-up transistor and a metal-programmable pull-down transistor, the metal-programmable transistor changing one or both of a range and a resolution of the set of available magnitudes when metal programmed, and

wherein the mode select input and the inverse mode select input control a selection between a weak write test mode (WWTM) and a default mode of operation of the bias generator, a set of selection inputs selecting the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic low level at the bias generator output in the default mode.